**AMENDMENTS TO THE SPECIFICATION**

**On page 3, approximately line 9, please delete the Heading "Description of Preferred Embodiments" and replace with:**

**DESCRIPTION OF EXEMPLARY EMBODIMENTS**

**On page 3, following the heading "Description of Exemplary Embodiments," please insert the following:**

Throughout the figures, certain reference characters are used to illustrate various exemplary aspects of the invention. The following reference characters are used in various figures: XX, NG, OK, $V_3$, $V_4$, $V_5$, PON, "0", EN, $V_{pp}$ and $V_{ppe}$. The previous reference characters are to be given the following non-limiting, exemplary meanings:

XX is an algebraic value held in the counter 20 prior to the counter 20 having received the "clear signal," CL. NG is a value of voltage that is not near enough to the exemplary voltage $V_{ppe}$ to be acceptable. OK is a value of voltage that is near enough to the exemplary voltage $V_{ppe}$ to be acceptable. $V_1$ through $V_7$ represent different voltages created by voltage divider 14 through resistors $R_1$ through $R_7$, respectively. PON is a power-on signal representing the fact that power has been turned on to the device. "0" (particularly as shown in Figure 6), illustrates the fact that the "EN" signal (enablement signal) is currently at a "zero" or "low" state. "EN" is a signal generated by the tester 200 that enables the generation of a sampling signal $S_2$ and a count-up (or count-down) signal $S_3$. $V_{pp}$ is a step-up (or step-down) voltage, and $V_{ppe}$ is an exemplary voltage against which $V_{pp}$ is compared. Further exemplary embodiments are both illustrated in the figures and described in the following written description.

**On page 3, please make the following changes to the paragraph beginning at line 18:**

The step-up voltage $V_{pp}$ of the step-up circuit 11 is determined by receiving a clock signal CLK via a NOR circuit 13. In this case, the step-up voltage $V_{pp}$ is controlled by a first feedback circuit FB1 connected between the step-up circuit 11 and the NOR circuit 13, so that the output voltage $V_i$ of [[the]] a selector 15 is brought close to the reference voltage $V_{ref}$ of [[the]] a reference voltage generating circuit 16. That is,

**On page 3, please make the following changes to the paragraph beginning at line 28:**

The first feedback circuit FB1 is formed by a voltage divider 14, [[a]] the selector 15, [[a]] the reference voltage generating circuit 16 and a comparator 17.

**On page 4, please make the following changes to the paragraph beginning at line 9:**

The selector 15 is constructed by eight switches 150, 151, ..., 157. Therefore, when the switches 150, 151, ..., 157, are respectively and individually[[,]] ~~is~~ turned ON, the step-up voltage $V_{pp}$ is brought close to:

**On page 4, please make the following changes to paragraph beginning at line 26:**

The selector 15 is controlled by a second feedback circuit FB2 connected between the output of the step-up circuit 11 and the selector 15, so that the step-up voltage $V_{pp}$ is brought close to an expected voltage $V_{ppe}$ from the tester 200. That is,

**On page 6, please make the following changes to the paragraph beginning at line 3:**

The adjustment operation of the nonvolatile semiconductor device 100 of Fig. 1 by the tester 200 will be explained next with reference to Fig. 2. Note that the value N of the counter 20 is indefinite before time $t_0$.

**On page 6, please make the following changes to the paragraph beginning at line 12:**

In this state (N = 0), the step-up voltage $V_{pp}$ is brought close to $V_0$ by the first feedback circuit FB1; that is, the counter 20 is at state N = 0, and this signal is fed to selector 15, which selectively chooses $V_0$ by closing the respectively associated switch (switch 150) so that $V_0$ becomes $V_{pp}$; however, the step-up voltage $V_{pp}$ is still below the expected value $V_{ppe}$, so that the comparison signal $S_1$ remains high ~~(= "1")~~(= "1").

**On page 6, please make the following changes to the paragraph beginning at line 22:**

In this state (N = 1), the step-up voltage $V_{pp}$ is brought close to $V_1$ by the first feedback circuit FB1; that is, the counter 20 is at state N = 1, and this signal is fed to selector 15, which selectively chooses $V_1$ by closing the respectively associated switch (switch 151) so that $V_1$ becomes $V_{pp}$; however, the step-up voltage $V_{pp}$ is still below the expected value $V_{ppe}$, so that the comparison signal $S_1$ remains high ~~(= "1")~~(= "1").

**On pages 6 and 7, please make the following changes to the paragraph bridging pages 6 and 7:**

In this state (N = 2), the step-up voltage $V_{pp}$ is brought close to $V_2$ by the first feedback circuit FB1; that is, the counter 20 is at state N = 2, and this signal is fed to selector 15, which selectively chooses $V_2$ by closing the respectively associated switch (switch 152) so that $V_2$

becomes $V_{pp}$; however, the step-up voltage $V_{pp}$ is still below the expected value $V_{ppe}$, so that the comparison signal $S_1$ remains high ~~(= "1")~~(= "1").

**On page 7, please make the following changes to the paragraph beginning at line 9:**

In this state (N = 3), the step-up voltage $V_{pp}$ is brought close to $V_3$ by the first feedback circuit FB1, so that the step-up voltage $V_{pp}$ exceeds the expected value $V_{ppe}$; that is, the counter 20 is at state N = 3, and this signal is fed to selector 15, which selectively chooses $V_3$ by closing the respectively associated switch (switch 153) so that $V_3$ becomes $V_{pp}$. Thus, the comparison signal $S_1$ is switched from high ("1") to low ~~(= "0")~~( = "0"), so that the step-up voltage $V_{pp}$ is brought close to the expected voltage $V_{ppe}$ by the second feedback circuit FB2.

**On pages 7 and 8, please make the following changes to the paragraph bridging pages 7 and 8:**

First, a power-on signal PON is generated from a control circuit (not shown) which also generates a read signal [[R]] RS and an address signal ADD indicating the adjustment area 12b. Therefore, the value "3" is transferred from the adjustment area 12b of the nonvolatile cell circuit 12 to the up counter 20. As a result, the step-up voltage $V_{pp}$ is brought close to $V_3$ by the first feedback circuit FB1. In this case, since the enable signal EN remains low (= "0") due to the presence of a resistor 191a, no sampling signal $S_2$ and no count-up signal $S_3$ are generated. Thus, the value "3" of the up counter 20 is unchanged.

**On page 8, please make the following changes to the paragraph beginning at line 8:**

In Fig. 1, a ~~resister~~ resistor 18a having a relatively large resistance is connected to a terminal to which the expected value $V_{ppe}$ is applied. As a result, in the post-adjustment

operation, since the expected value $V_{ppe}$ is 0V, the generation of count-up signals can be further suppressed, which more surely ~~prevent~~ prevents a change in the value of the counter 20.

**On page 9, please make the following changes to the paragraph beginning at line 13:**

The adjustment operation of the nonvolatile semiconductor device 100' of Fig. 4 by the tester 200' will be explained next with reference to Fig. 5. Note that the value N of the counter 20' is indefinite before time $t_0$.

**On page 9, please make the following changes to the paragraph beginning at line 22:**

In this state (N = 7), the step-up voltage $V_{pp}$ is brought close to $V_7$ by the first feedback circuit FB1; that is, the counter 20 is at state N = 7, and this signal is fed to selector 15, which selectively chooses $V_7$ by closing the respectively associated switch (switch 157) so that $V_7$ becomes $V_{pp}$; however, the step-up voltage $V_{pp}$ is still higher than the expected value $V_{ppe}$, so that the comparison signal $S_1$ remains high ~~(= "1")~~ (= "1").

**On pages 9 and 10, please make the following changes to the paragraph bridging pages 9 and 10:**

In this state (N = 6), the step-up voltage $V_{pp}$ is brought close to $V_6$ by the first feedback circuit FB1; that is, the counter 20 is at state N = 6, and this signal is fed to selector 15, which selectively chooses $V_6$ by closing the respectively associated switch (switch 156) so that $V_6$ becomes $V_{pp}$; however, the step-up voltage $V_{pp}$ is still higher than the expected value $V_{ppe}$, so that the comparison signal $S_1$ remains high ~~(= "1")~~ (= "1").

**On page 10, please make the following changes to the paragraph beginning at line 9:**

In this state (N = 5), the step-up voltage $V_{pp}$ is brought close to $V_5$ by the first feedback circuit FB1; that is, the counter 20 is at state N = 5, and this signal is fed to selector 15, which

selectively chooses $V_5$ by closing the respectively associated switch (switch 155) so that $V_5$ becomes $V_{pp}$; however, the step-up voltage $V_{pp}$ is still higher than the expected value $V_{ppe}$, so that the comparison signal $S_1$ remains high ~~(= "1")~~ (= "1").

**On page 10, please make the following changes to the paragraph beginning at line 19:**

In this state (N = 4), the step-up voltage $V_{pp}$ is brought close to $V_4$ by the first feedback circuit FB1, so that the step-up voltage $V_{pp}$ is below expected value $V_{ppe}$; that is, the counter 20 is at state N = 4, and this signal is fed to selector 15, which selectively chooses $V_4$ by closing the respectively associated switch (switch 154) so that $V_4$ becomes $V_{pp}$. Thus, the comparison signal $S_1$ is switched from high ("1") to low ~~(="0")~~ (= "0"), so that the step-up voltage $V_{pp}$ is close to the expected voltage $V_{ppe}$.

**On page 10, please make the following changes to the paragraph beginning at line 25:**

As a result, upon receipt of the change of the comparison signal $S_1$, the tester 200' stops the generation of the enable signal EN, so that the sampling signal $S_2$ and the ~~count-up signal $S_3$~~ count-down signal $S_3'$ are no longer generated. Thus, the adjustment of the value N of the down counter 20' is completed, i.e., the value N of the down counter 20' is fixed at "4".

**On page 11, please make the following changes to the first and second full paragraphs:**

The post-adjustment operation of the nonvolatile semiconductor memory device of Fig. [[3]] 4 will be explained next with reference to Fig. 5. Here, assume that the value "3" is stored in adjustment area 12b of the nonvolatile cell circuit 12.

First, a power-on signal PON is generated from a control circuit (not shown) which also generates a read signal [[R]] RS and an address signal ADD indicating the adjustment area 12b. As a result, the value "4" is set from the adjustment area 12b of the nonvolatile cell circuit 12 to the down counter 20'. As a result, the step-up voltage $V_{pp}$ is brought close to $V_4$ by the first feedback circuit FB1. In this case, since the enable signal EN remains low (= "0") due to the presence of a resistor 191a, no sampling signal $S_2$ and no count-down signal $S_3$' are generated. Thus, the value "4" of the down counter 20' is unchanged.

## AMENDMENTS TO THE DRAWINGS

Submitted herewith please find six (6) sheets of replacement drawings in compliance with 37 C.F.R. § 1.84. The Examiner is respectfully requested to acknowledge receipt of these drawings.

Attachment: 6 Replacement Sheets (Figures 1 - 6)